REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 18-20 and 24-25 stand rejected under 35 U.S.C. §112, second paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. As to claim 18, it is alleged that the language "the low speed arbiter supports a lower bus rate than the high speed bus arbiter" is unclear. Applicants note that page 4, lines 5-10 of the Specification and elsewhere support this subject matter and it was also in originally filed claim 18. Applicants respectfully submit that the rejection be withdrawn.

Claims 18-20, 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Iachetta Jr. in view of Porterfield, Ajanovic, and Heil et al. The claims describe a structure for example that, among other advantages, allow for the servicing of a data storage medium such as a hard drive or other storage medium via a bus other than for example, a PCI bus or other system bus, and servicing the I/O controller via a high speed bus such as a high speed PCI bus so that accessing data from the hard drive is done without limiting the bandwidth on the low speed PCI bus interface. The high-speed PCI interface can allow for high speed data storage access either from the hard drive or the external PCI devices. (See e.g., Specification page 3). Claim 18 requires, inter alia, that the input-output controller which is in communication with the high speed bus arbiter via the high speed bus, includes a low speed bus arbiter coupled to a low speed bus and also includes a separate bus that is instead coupled to a data storage device. Claim 24 also requires similar limitations in that the data storage device which is coupled to the I/O controller is coupled thereto via a different bus to transmit data at a higher rate than the data rate of the low speed bus arbiter which is in the I/O controller. As such, applicants respectfully

submit that the claims are in condition for allowance. The Iachetta reference suffers from the same problems as the prior art wherein the low speed arbiter is a bottleneck for the data going to the devices coupled to the low speed bus. The final office action does not appear to address this language regarding the I/O controller with separate bus and low speed arbiter and the cited portions of the referenced do not describe the claimed subject matter. Applicant respectfully submits that these claims are in condition for allowance.

Claim 25 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Iachetta Jr. in view of Porterfield and Ajanovic, and Heil et al. as applied to claims 18-20 above and further in view of "Wikipedia cited below". The claim requires a dual bus based unified memory architecture wherein a unified memory is controlled to store both graphics data and system data, in combination with other limitations and is at least allowable as depending on an allowable base claim.

The dependent claims add additional novel and non-obvious subject matter.

Accordingly, Applicants respectfully submit that the claims are now in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

<div align="center">Respectfully submitted,</div>

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